

**CLAIMS**

What is claimed is:

1. A method of fabricating a shallow trench isolation feature comprising the steps of:
  - providing a semiconductor substrate;
  - forming a polish stop layer over the semiconductor substrate;
  - forming a nitride containing layer over the polish stop layer;
  - forming a shallow trench layer through a portion of the nitride containing layer, a portion of the polish stop layer and a portion of the semiconductor substrate;
  - removing the nitride containing layer by a chemical mechanical polishing process; and
  - planarizing the shallow trench layer and the polish stop layer until a surface of the shallow trench layer and a surface of the polish stop layer are co-planar.
2. A method according to claim 1, including the step of:
  - forming a barrier layer over the semiconductor substrate.
3. A method according to claim 1, including the step of:
  - etching an aperture through the nitride containing layer to expose a portion of the polish stop layer.
4. A method according to claim 1, including the steps of:
  - forming a shallow trench through a portion of the polish stop layer and a portion of the semiconductor substrate; and
  - depositing an oxide in the shallow trench to form the shallow trench layer.
5. A method according of claim 1, wherein the polish stop layer is at least one of polysilicon and silicon carbide.
6. A method according to claim 5, wherein the polish stop layer is polysilicon.

7. A method according to claim 6, including the step of:  
oxidizing the polish stop layer to convert the polysilicon to a field oxide layer.
8. A method according to claim 3, wherein the nitride containing layer is at least one of  $\text{Si}_3\text{N}_4$  and  $\text{SiO}_x\text{N}_y$ .
9. A method according to claim 1, including the step of:  
forming a liner layer interposed between the shallow trench layer and the semiconductor substrate.
10. A shallow trench isolation feature comprising:  
a semiconductor substrate;  
a polish stop layer formed over the semiconductor substrate; and  
a shallow trench layer formed through a portion of the polish stop layer and a portion of the semiconductor substrate;  
wherein a surface of the shallow trench layer and a surface of the polish stop layer are co-planar.
11. The shallow trench isolation feature according to claim 1, including:  
a barrier layer formed over the semiconductor substrate.
12. A shallow trench isolation feature according to claim 1, including:  
a shallow trench formed through a portion of the polish stop layer and a portion of the semiconductor substrate.
13. A shallow trench isolation feature according to claim 1, wherein the polish stop layer is at least one of polysilicon and silicon carbide.
14. A shallow trench isolation feature according to claim 13, wherein the polish stop layer is polysilicon.
15. A shallow trench isolation feature according to claim 14, wherein a field oxide layer is formed from the polish stop layer.

16. A shallow trench isolation feature according to claim 1, including:  
a liner layer interposed between the shallow trench isolation layer and the semiconductor substrate.
17. A shallow trench isolation feature according to claim 16, including the liner layer interposed between the shallow trench isolation layer and the barrier layer.
18. A shallow trench isolation feature according to claim 17, including:  
a liner layer interposed between the shallow trench isolation layer and the polish stop layer.
19. A semiconductor device comprising:  
a transistor formed on a semiconductor substrate; and  
at least one shallow trench isolation feature including:  
a polish stop layer formed over the semiconductor substrate;  
a shallow trench layer formed through a portion of the polish stop layer and a portion of the semiconductor substrate;  
wherein a surface of the shallow trench layer and a surface of the polish stop layer are co-planar.
20. A semiconductor device according to claim 19;  
wherein the polish stop layer is one or more of polysilicon and silicon carbide.